Wenjie Xiong

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Education

Yale University **New Haven, CT, USA**
Ph.D. Candidate & Master of Science in Electrical Engineering *Aug. 2014 – present*
Department of Electrical Engineering
Advisor: Prof. Jakub Szefer
Courses: Computer Architecture; Cryptography; Information Theory; Database; Cloud Computing; Linear Systems.

Peking University **Beijing, China**
Bachelor of Science in Microelectronics *Sep. 2010 – Jul. 2014*
School of Electronics Engineering and Computer Science
Cumulative GPA: **3.76/4.0** (Rank: **4/45**), *Major GPA:* **3.86/4.0** (Rank: **3/45**)
Courses:
Electrical Engineering – Signals and Systems; Semiconductor Physics; Semiconductor Device Physics; Principle of Digital/ Analog Integrated Circuits; ICCAD; Advanced Analog IC Design; RF IC;
Computer Science – Programming in C&C++; Data Structure and Algorithm; Principle of Microcomputer;
Physics – Mechanics; Electromagnetism; Thermal; Optics;
Mathematics – Mathematical Analysis; Advanced Algebra; Probability Theory and Statistics.

Peking University **Beijing, China**
Bachelor of Science in Psychology *Sep. 2010 – Jul. 2014*
Department of Psychology
Courses: Experimental, Cognitive, Social, Abnormal, and Developmental Psychology; Central Nervous System Anatomy.

Research Experience

Computer Architecture and Security Laboratory (CASLab), Yale University *Aug. 2014 – present*

Practical DRAM PUF in Commodity Devices and its Application
Advisor: Prof. Jakub Szefer, Prof. Stefan Katzenbeisser (TU Darmstadt, Germany)
- Demonstrated a novel type of PUFs (physical unclonable functions) using DRAM (Dynamic Random Access Memory)
- implemented two practical DRAM PUF access methods in firmware as well as a Linux kernel module in Intel Galileo and Pandaboard
- Designed new authentication and key storage scheme based on DRAM PUFs
- Exploited inherent DRAM features for advanced cryptographic protocols
- Improved the PUF readout time with row hammer effect

Security Verification of Processor Architectures
Advisor: Prof. Jakub Szefer, Prof. Onur Demir (Yeditepe University, Turkey)
- Developing new ways to model hardware and verify the security of processor architectures by adding new annotations in hardware description language, leveraging current functional verification tools, e.g. Coq.

Design and Simulation of Secure Architecture with DIFT
Advisor: Prof. Jakub Szefer
- Design and simulate a secure architecture with Dynamic Information Flow Tracking (DIFT) to protect database
- Implement information flow tracking features into GEM5, which is an open-source simulator
- Test and evaluate the DIFT approach to database computation protection
- Modified two applications, SQLite and Redis, to demonstrate the usability of the architecture

Institute of Microelectronics, Peking University *Apr. 2012 – Jun. 2014*

Design of Neural Stimulation System for Insect Cyborg (senior project)

Advisor: Prof. Zhihong Li

- A new design of neural stimulation system for insect flight control.
- Designed and simulated the circuit, including digital logic, DC-DC converter, and output array in Cadence IC.

Design, Simulation, Fabrication and Test of cuff electrodes

Advisor: Prof. Zhihong Li

- Built 3D finite element model and Simulated electric field distribution of working cuff electrodes in COMSOL
- Fabrication: photolithography, oxygen plasma etching, wet etching of Si, SiO_2 and metals, Ni and Au electroplating

Teaching Experience

EENG 201 Teaching Assistent, Introduction to Computer Engineering, Yale University *2016 Spring*
EENG 201 Teaching Assistent, Introduction to Computer Engineering, Yale University *2017 Spring*
Topics include boolean algebra, digital design, and basic computer architecture principles. I assisted Prof. Szefer in preparing lab materials, leading lab sessions, and grading.

Working Experience

Intel Labs Security Research Intern *Jun.- Aug. 2017*
Data integrity with minimal bandwidth overhead. Evaluated bandwidth overhead of real-world workloads with functional simulator. Implemented algorithms in RTL and evaluated delay and area overhead.

Selected Publications

- A. Schaller, **W. Xiong**, M. U. Saleem, N. A. Anagnostopoulos, S. Katzenbeisser and J. Szefer, "Intrinsic Rowhammer PUFs: Leveraging the Rowhammer Effect for Improved Security" *in Proceedings of the International Symposium on Hardware Oriented Security and Trust (HOST)*, May 2017. (Best Student Paper Finalist)
- O. Demir, **W. Xiong**, F. Zaghloul, and J. Szefer, "Survey of Approaches for Security Verification of Hardware/Software System", *Cryptology ePrint Archive*, Report 2016/846, (2016).
- **W. Xiong**, A. Schaller, N. A. Anagnostopoulos, M. U. Saleem, S. Gabmeyer, S. Katzenbeisser and J. Szefer, "Run-time Accessible DRAM PUFs in Commodity Devices," *Cryptographic Hardware and Embedded Systems (CHES)*, (2016).
- H. Yu, **W. Xiong**, H. Zhang, W. Wang and Z. Li, "A Parylene Self-Locking Cuff Electrode for Peripheral Nerve Stimulation and Recording" *Journal of Microelectromechanical Systems* **23**, (2014).

Selected Honors and Awards

- Microsoft Research Graduate Women's Scholars 2015
- National Scholarship, China 2013
- Merit Student of Peking University 2012
- Wusi Scholarship of Peking University 2011
- Merit Student of Zhejiang Province 2010
- First Prize of High School Biology Olympiad, Zhejiang Province, China 2009

Skills

- Programming languages: C/C++, Python, MATLAB, Verilog, VHDL, SQL, Bash