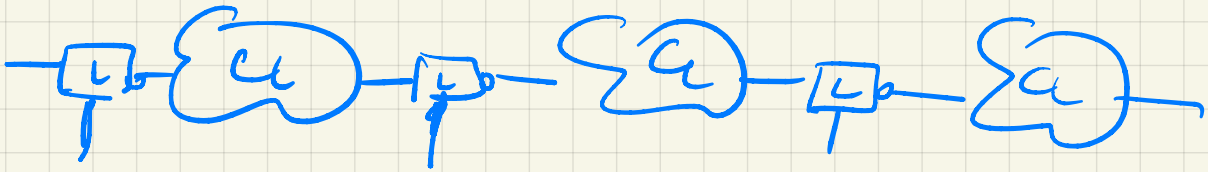
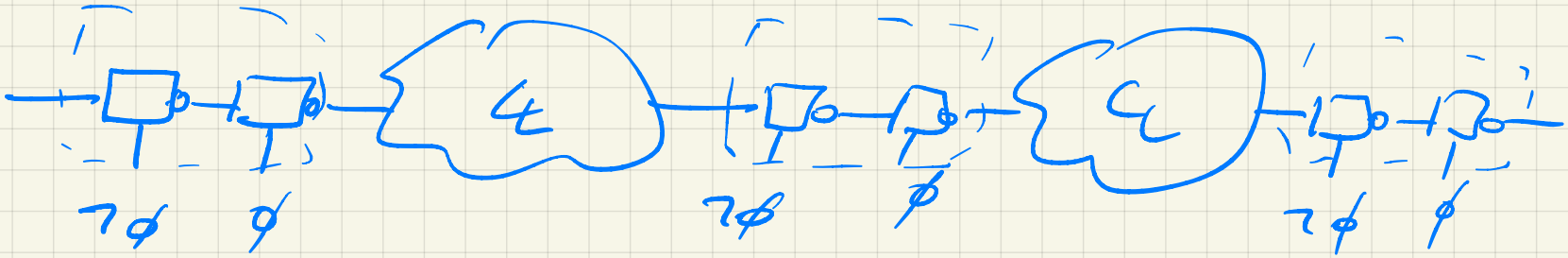
Clocking

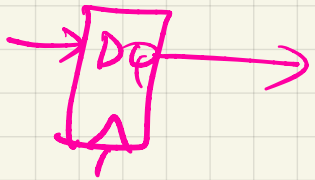
Single phase



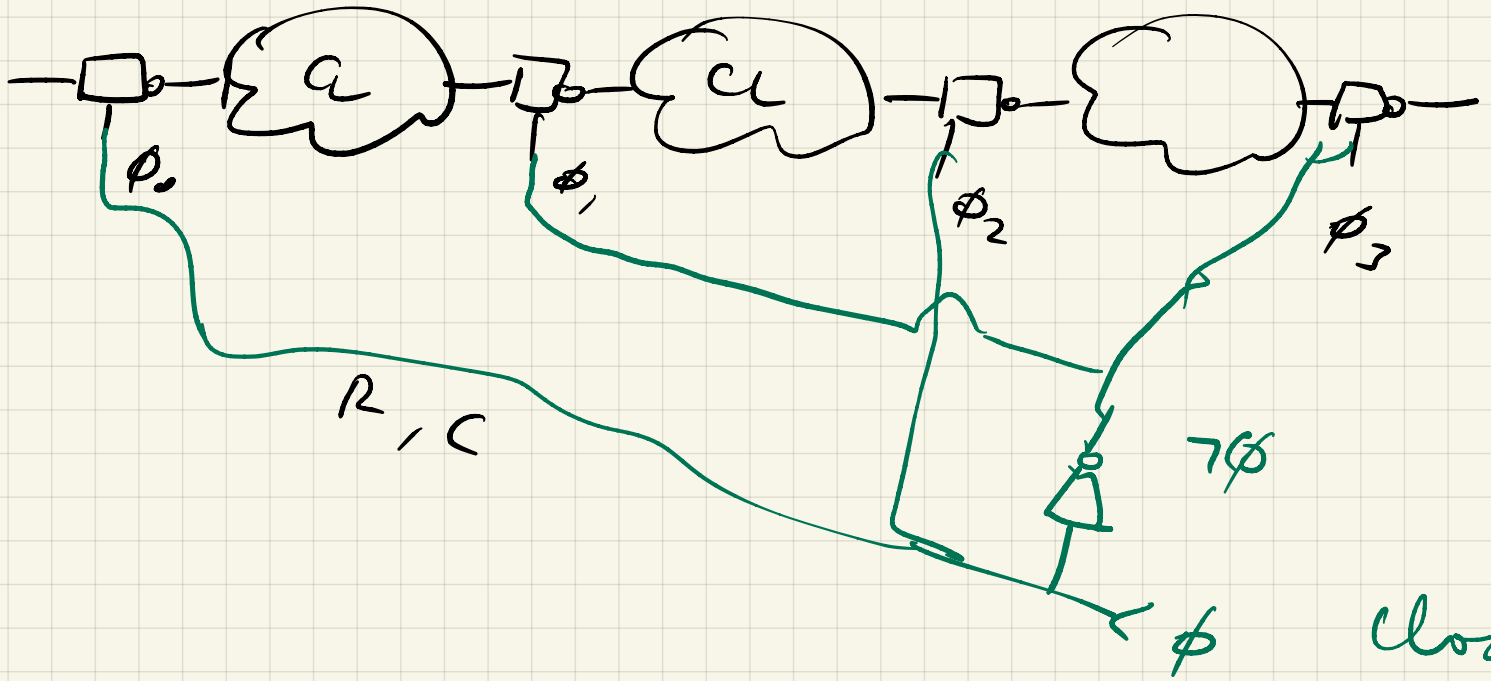
single phase { ϕ ϕ ϕ / ϕ $\neg\phi$ ϕ

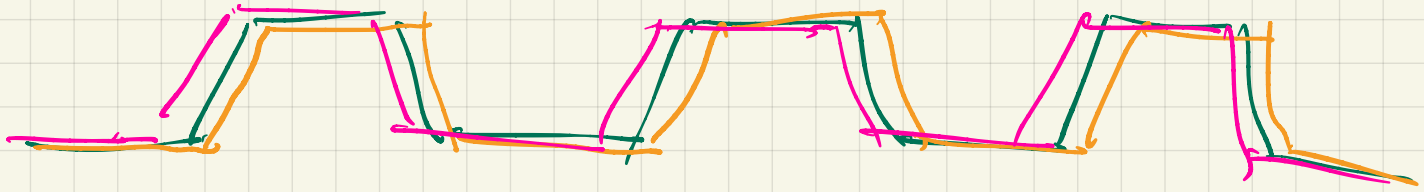
2-phase non-overlapping { ϕ_0 ϕ_1 ϕ_0





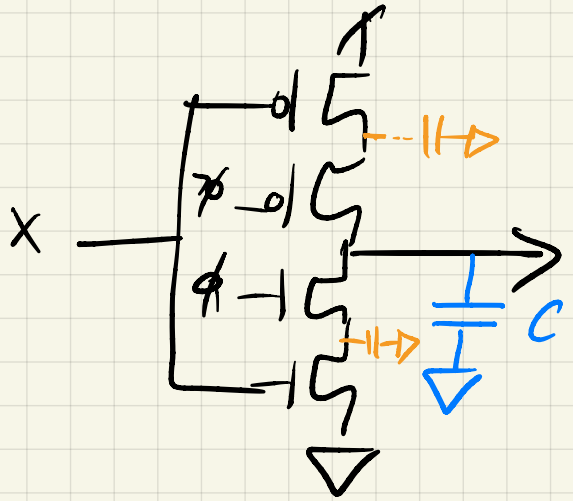
φ clk

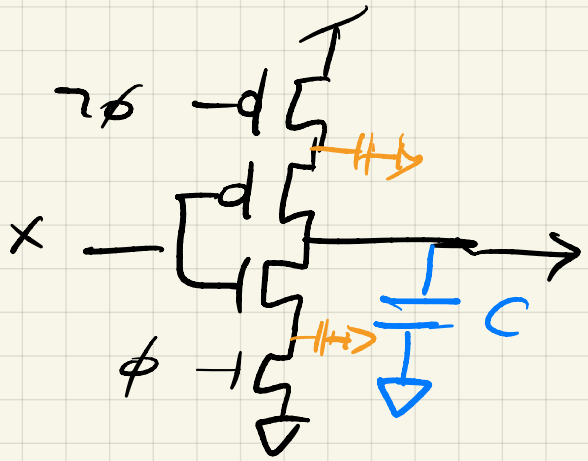




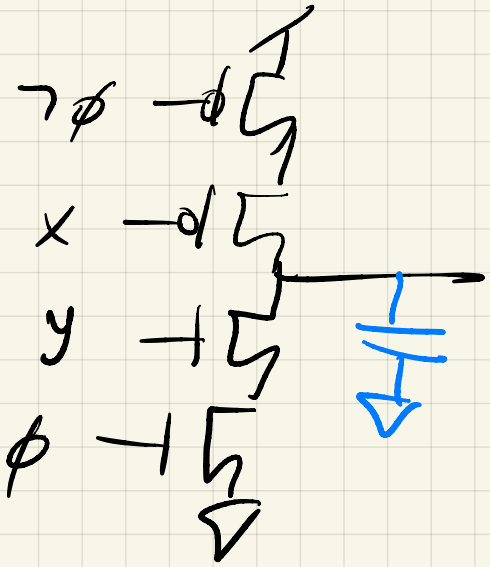
launching clock;

clock skew $\rightsquigarrow$ useful skew

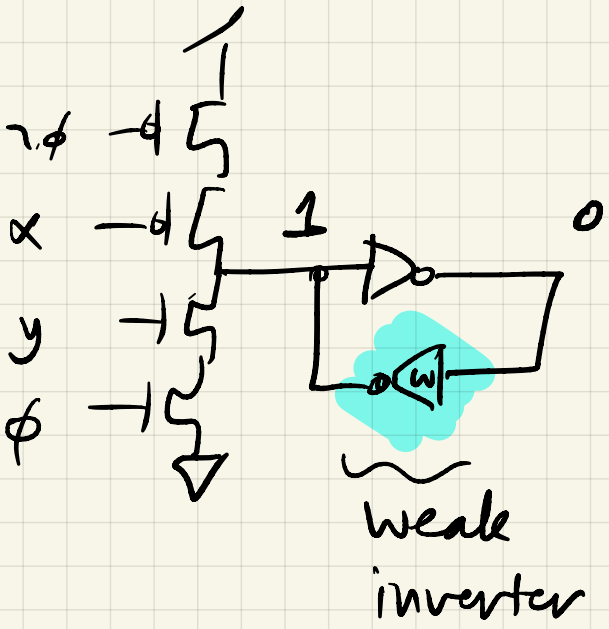


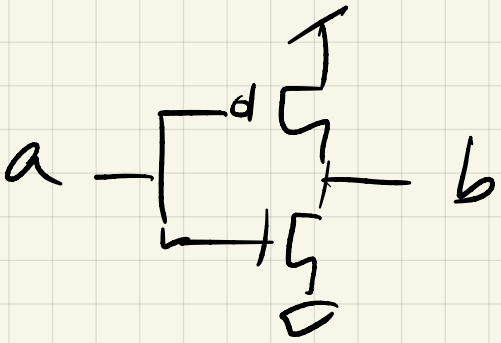


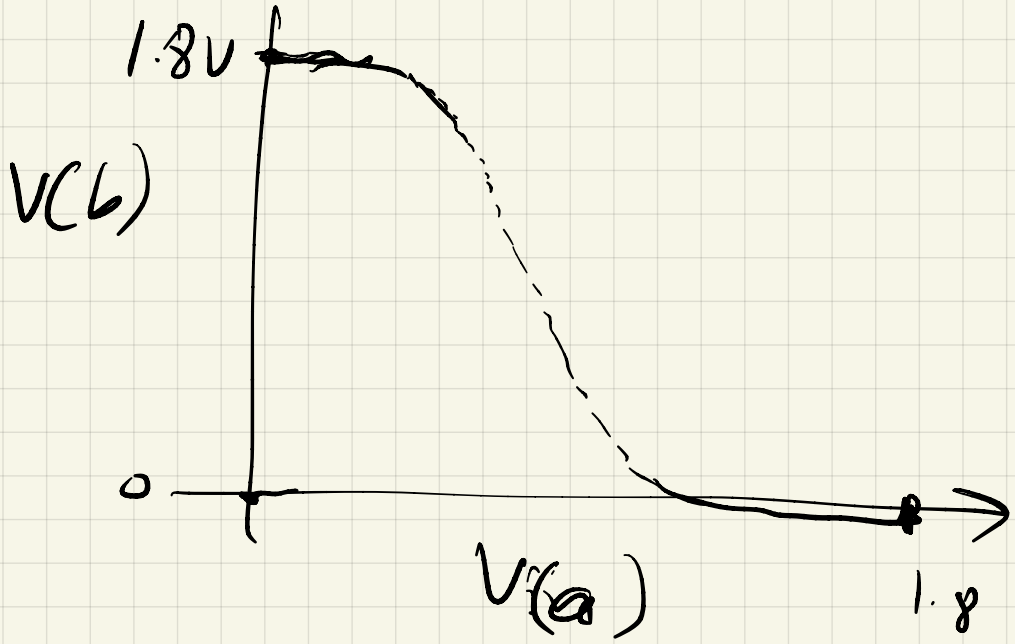
Charge-sharing:

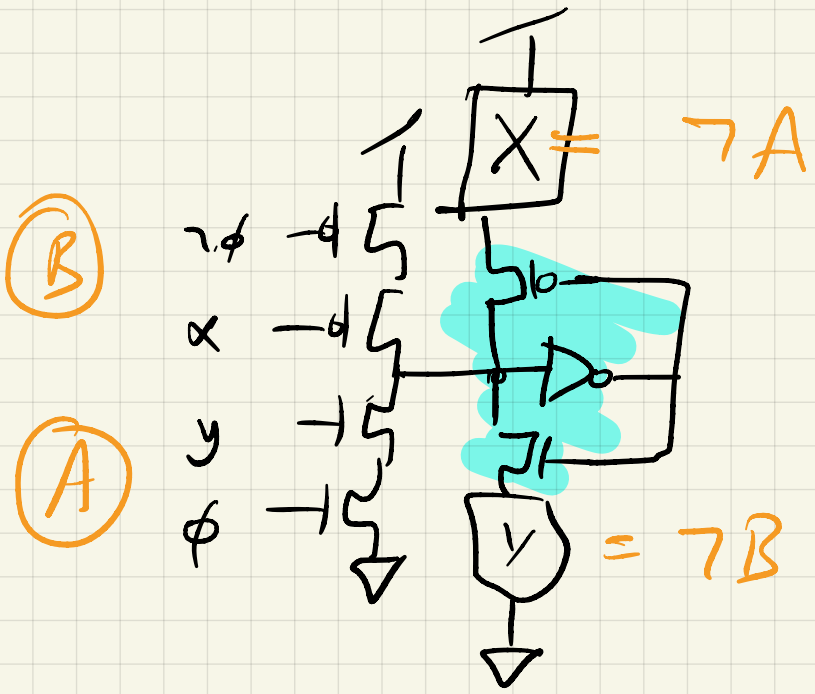


} Charge pumping.


1
0
weak
inverter

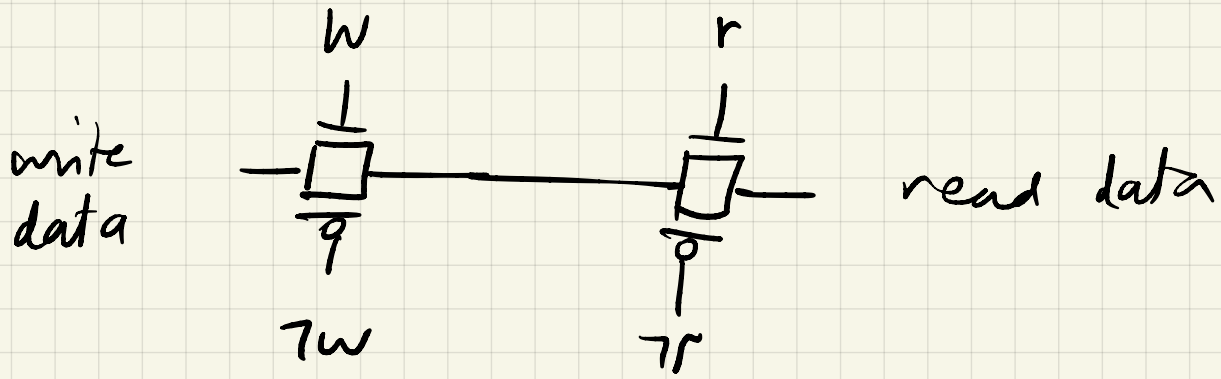

a
b


1.8V
V(b)
0
V(a)
1.8

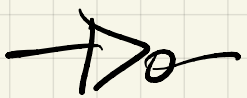


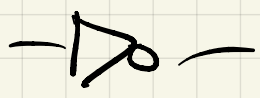
combinational feedback.

Single port register



① Add inverters: <u>direction</u> to read & write


write


read