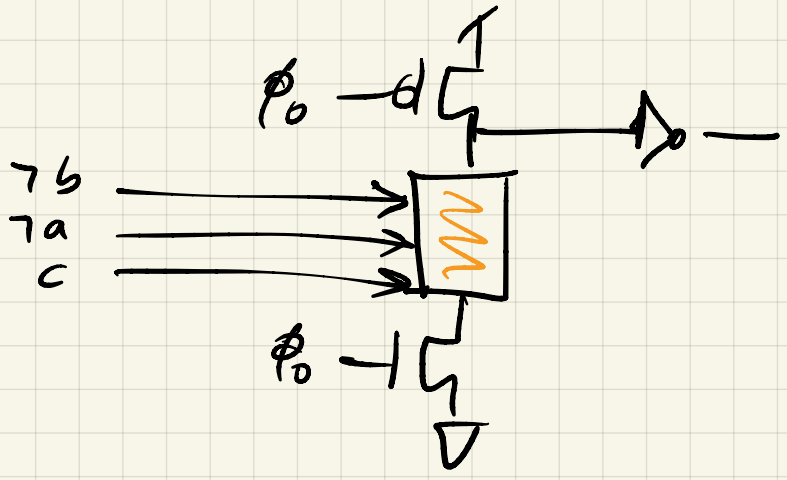
Precharge Logic + Retiming

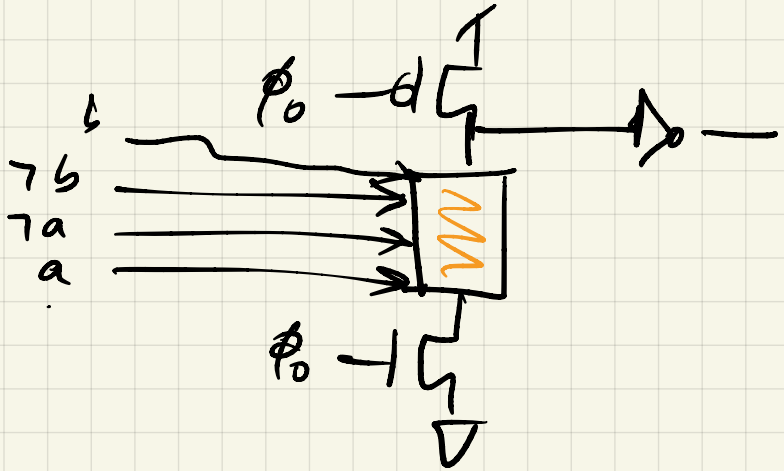
NAND-OR

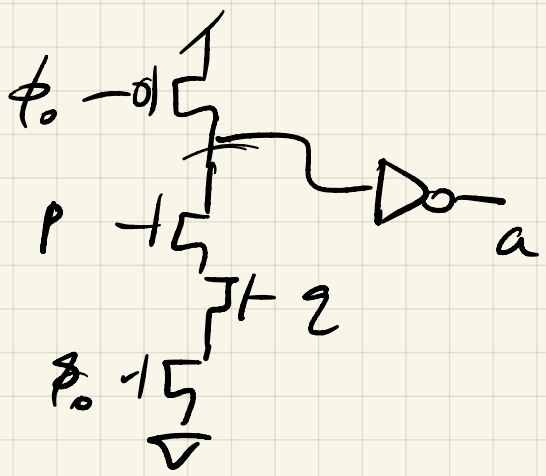
$\neg(a \wedge b) \vee c$ $\quad \overline{ab} + c$

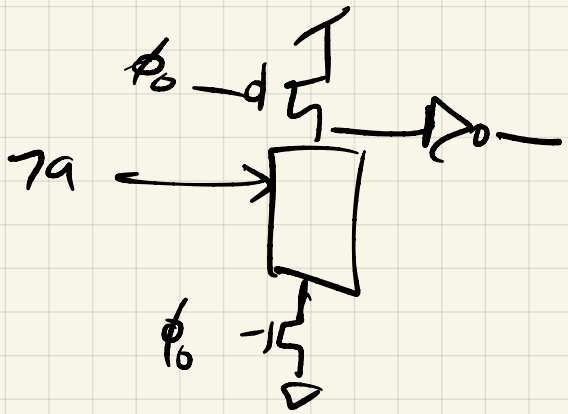
$\neg a \vee \neg b \vee c$



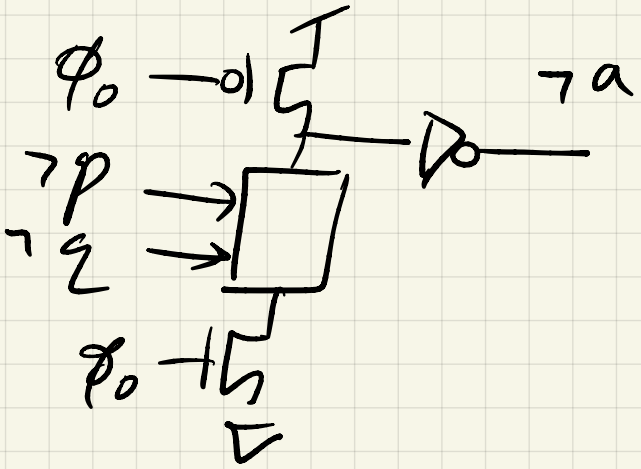
XOR (a, b) $\quad (\neg a \wedge b) \vee (a \wedge \neg b)$ $\quad a, \neg a$ $b, \neg b$

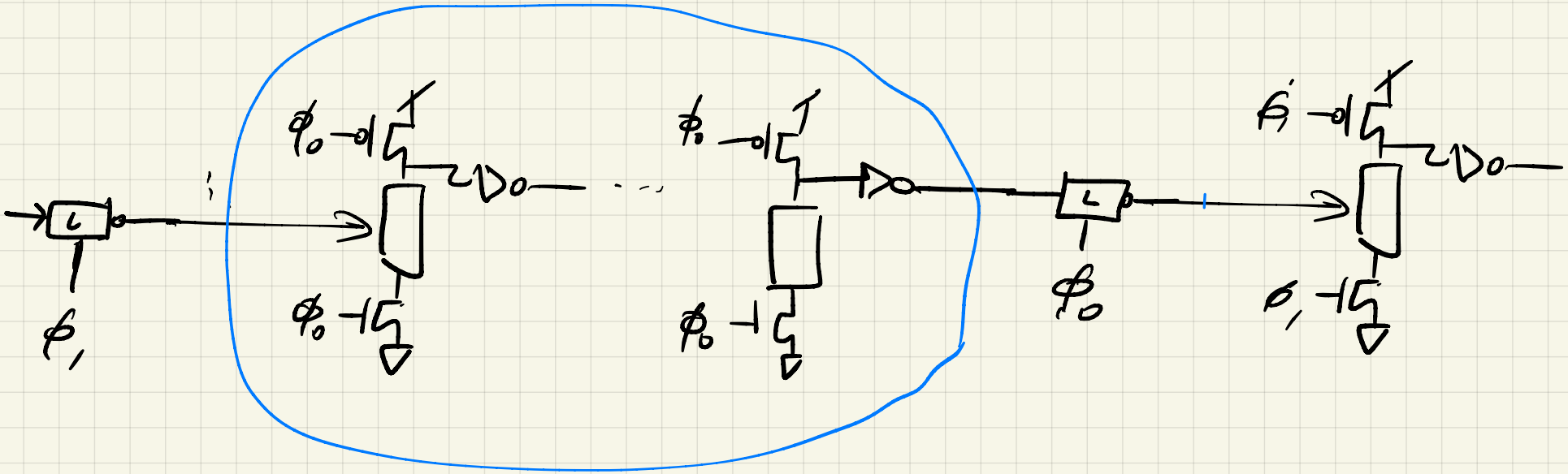




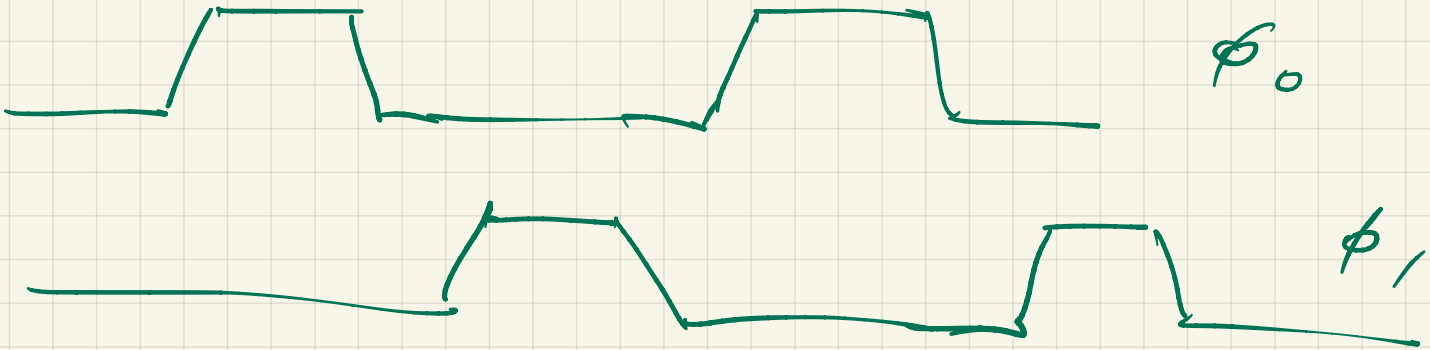


$$p \wedge q \rightsquigarrow \neg(p \wedge q) = \neg p \vee \neg q$$

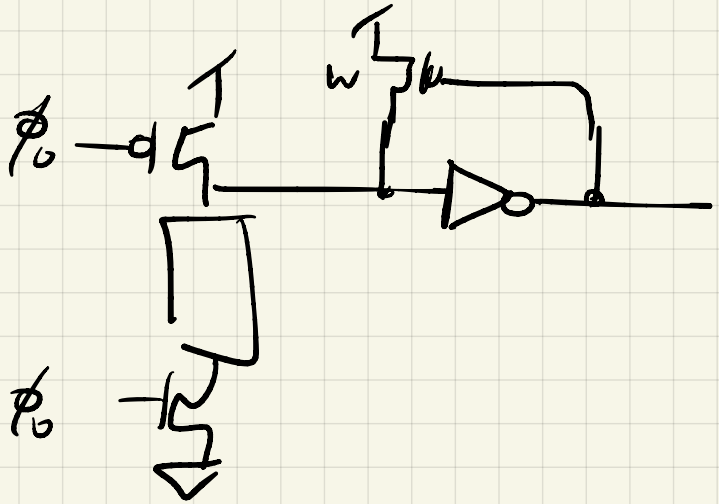




pre-charge logic

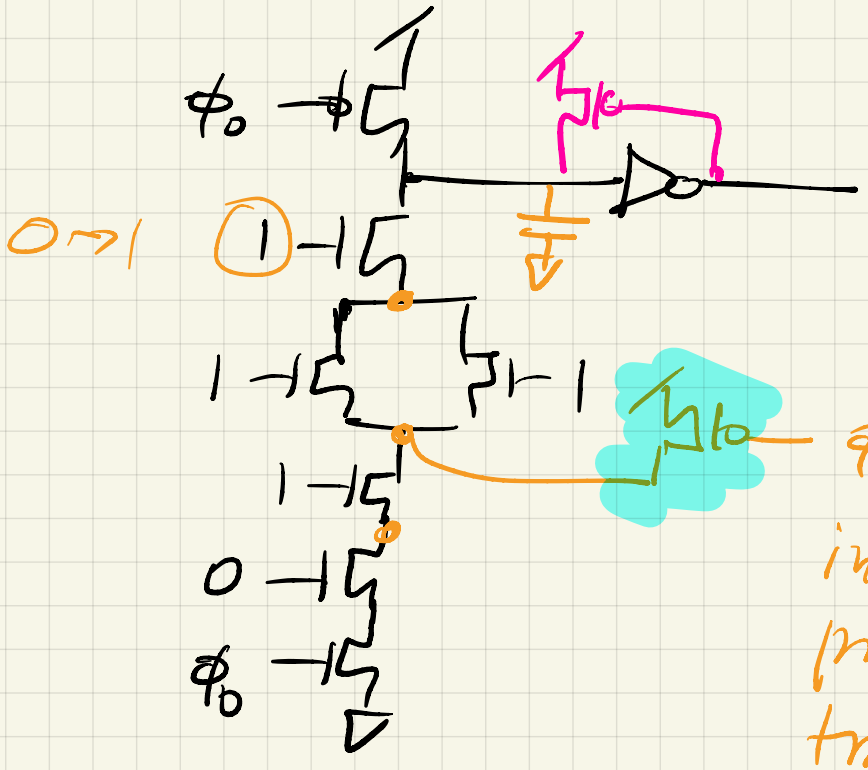


domino logic

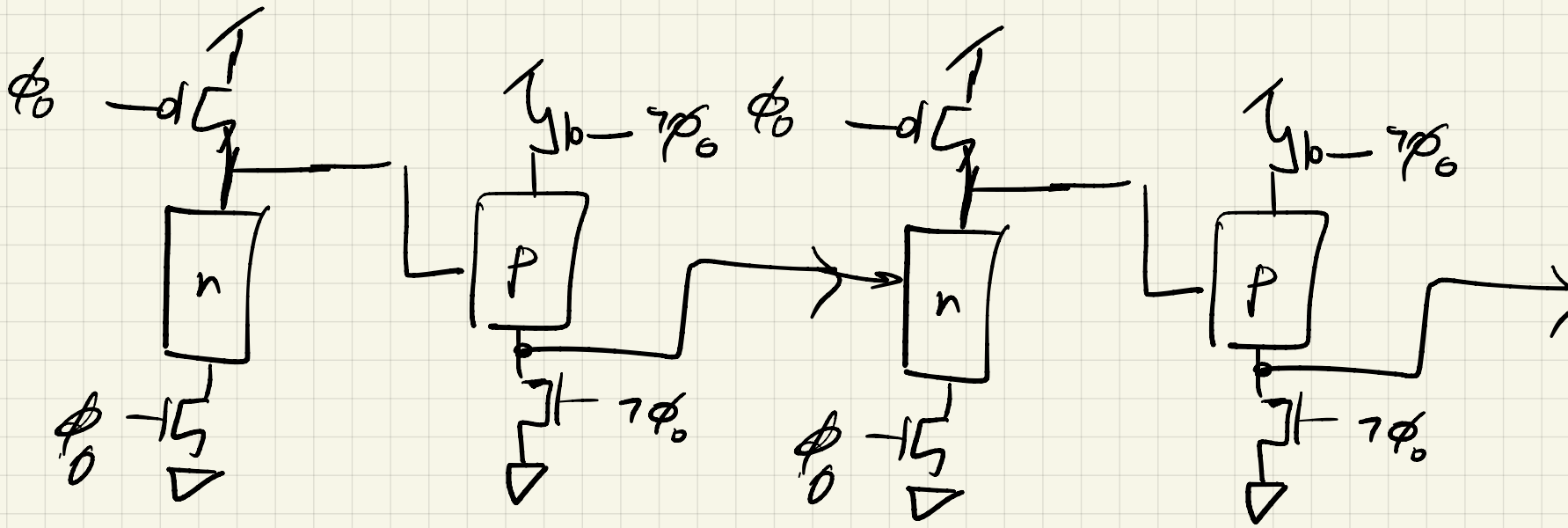


half-staticizer

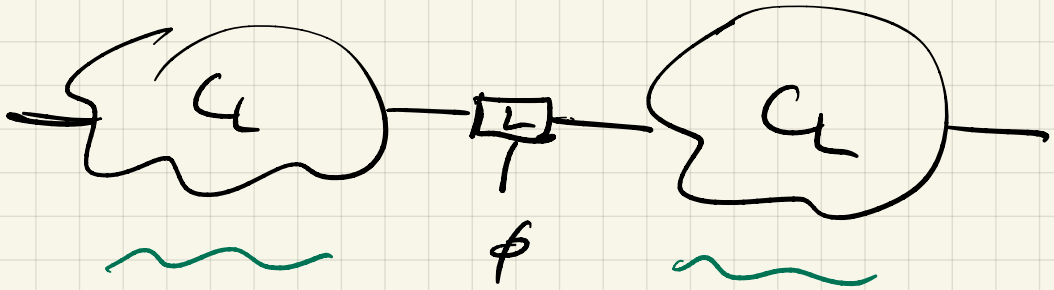
staticize high only

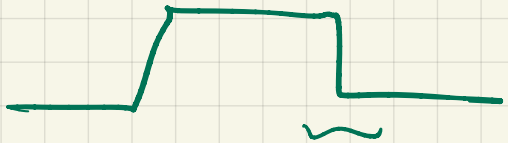


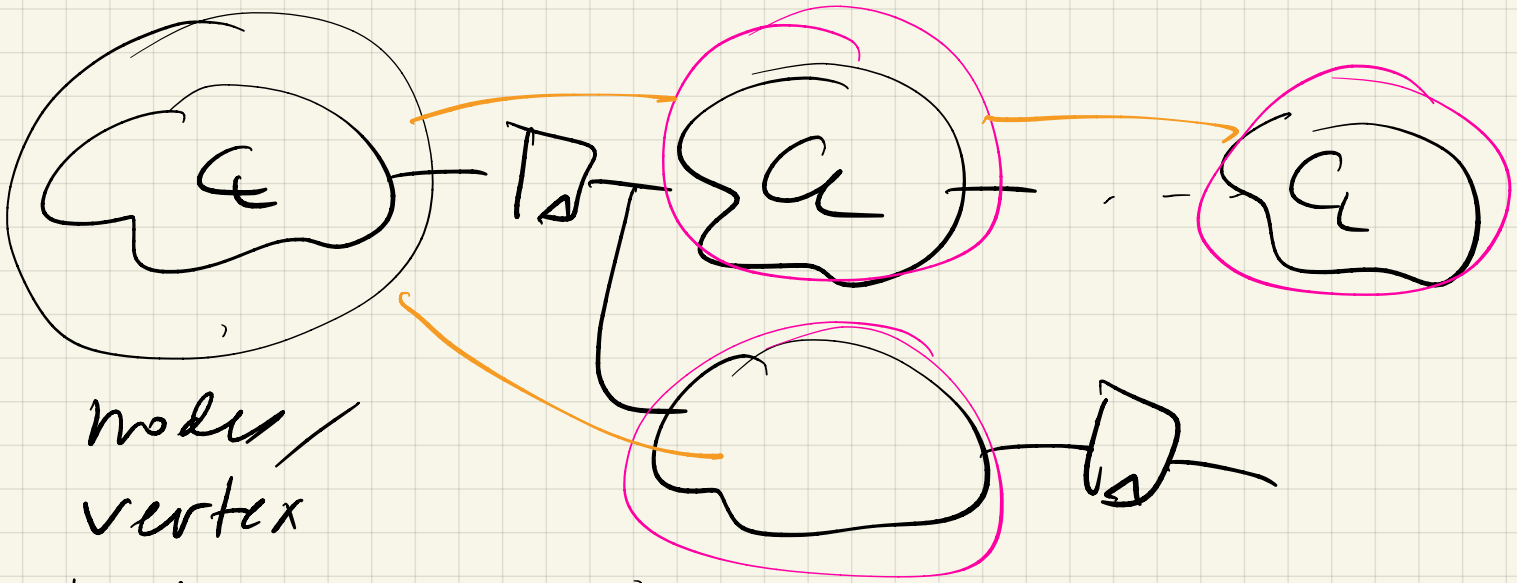
Charge-sharing in precharge logic.



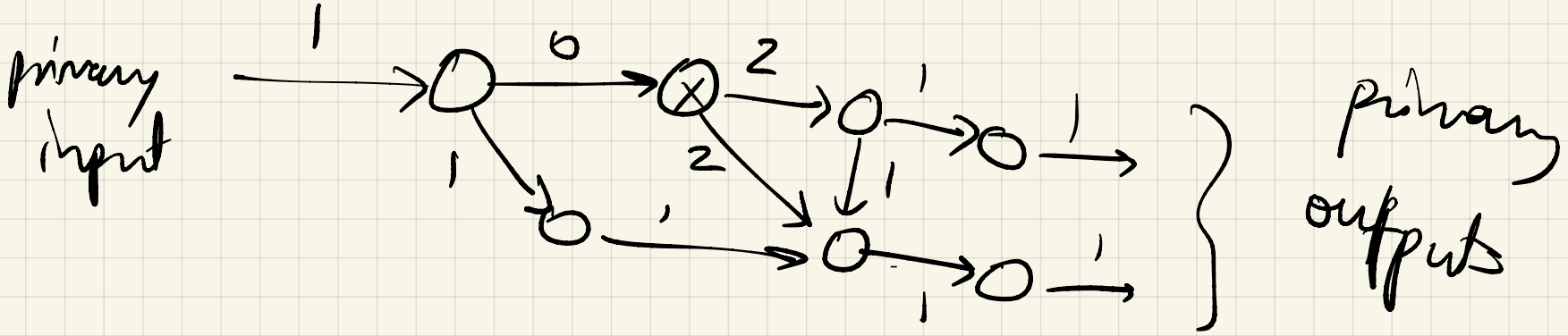
n-p domino logic.

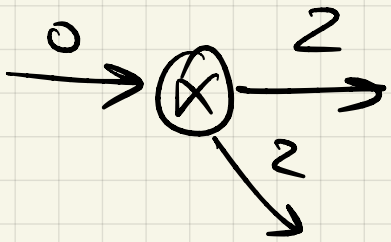


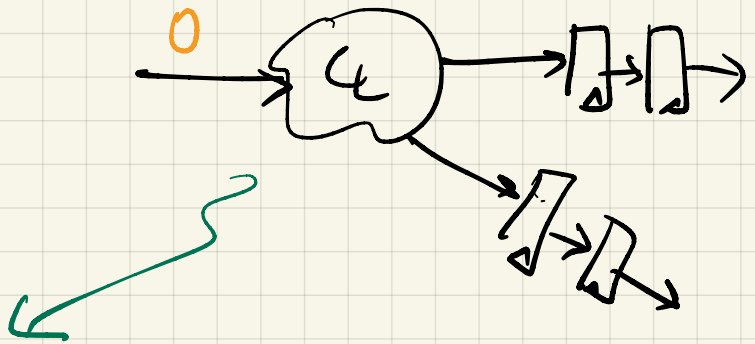


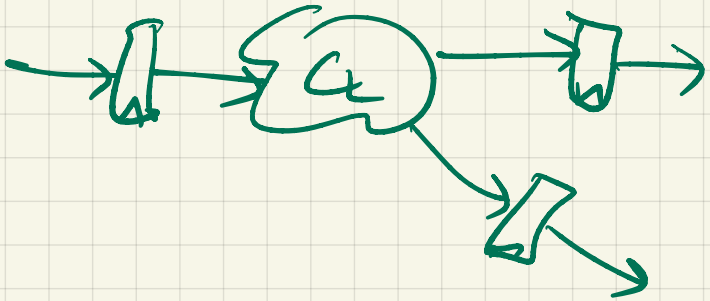


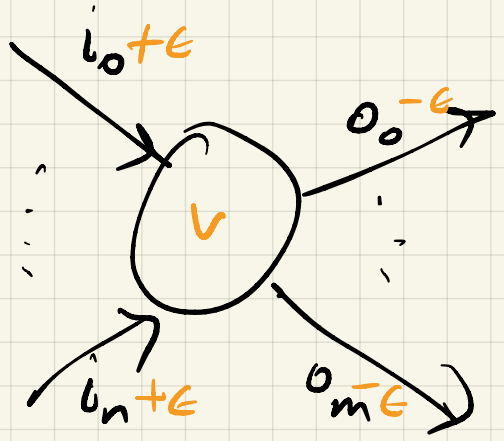
node / vertex in the graph


primary input
1
0
2
1
2
1
1
1
1
1
1
1
primary outputs


0
2
2


0





$\delta(v) = \epsilon$

$lag(v)$